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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,060	03/12/2004	Jeffrey W. Lutze	SNDK.352US0	6740

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PARSONS HSUE & DE RUNTZ LLP
655 MONTGOMERY STREET
SUITE 1800
SAN FRANCISCO, CA 94111

EXAMINER	
TRAN, MAI HUONG C	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/799,060	LUTZE ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *19-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/24/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Application's election without traverse of Group II (Claims 1-18) drawn to a semiconductor device is acknowledged for prosecution in the subject application. Accordingly, claims 19-22 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicants have the right to file a divisional application covering the subject matter of the non-elected claims.

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,559,008 to Rabkin et al. in view of Patelmo et al. (US 6,281,077).

Regarding to claims 1-10, Rabkin discloses a method of forming an array of non-volatile memory cells on a semiconductor substrate surface, comprising forming a plurality of shallow trench isolation structures spaced apart across the surface of a substrate in a first direction and extending in a second direction, individual shallow trench isolation structures having sidewalls that extend vertically from the substrate surface; forming a plurality of floating gate structures, individual floating gate structures extending between a first sidewall of a first shallow trench isolation structure and a second sidewall of a second shallow trench isolation structure and being bounded in a first direction by the first and second sidewalls (cols. 1-8 and figs. 1-5).

Rabkin does not disclose shaping the plurality of floating gate structures to reduce the width in a second direction of an upper part of individual ones of the plurality of floating gate structures.

However, Patelmo et al. teach shaping the plurality of floating gate structures to reduce the width in a second direction of an upper part of individual ones of the plurality of floating gate structures (col. 4, lines 36-67, col. 5, and figs. 10-18).

It would have been obvious to one of ordinary skill in the art at the time the inventionwas made to form shaping the plurality of floating gate structures to reduce the width in a second direction of an upper part of individual ones of the plurality of floating gate structures, as taught by Patelmo in order to provide a method for manufacturing non-volatile cells and high-speed transistors with a small number of masks, which is simple, and has the lowest possible costs (col. 1, lines 50-54).

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 11-18 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,559,008 to Rabkin et al.

Regarding to claims 11-14, Rabkin et al. discloses a method of forming an array of non-volatile memory cells on a semiconductor substrate surface, comprising forming a plurality of structures having sidewalls that extend from the substrate surface; forming a plurality of conductive strips, an individual conductive strip extending between a first sidewall and a second sidewall of the plurality of structures having sidewalls, an individual conductive strip bounded by the first and second sidewalls; forming a plurality of separate floating gate structures by removing portions of the plurality of conductive strips, removed portions extending from a first sidewall to a second sidewall (cols. 1-8 and figs. 1-5).

Regarding to claims 15-18, Rabkin et al. disclose a method of forming an array of non-volatile memory cells on a semiconductor substrate surface, comprising forming a first plurality of conductive strips that are separated in a first direction, that extend across the substrate surface in a second direction and that have protrusions extending in a direction away from the substrate surface with recesses between protrusions; forming a dielectric layer overlying the first plurality of conductive strips; forming a conductive layer over the dielectric layer; and etching portions of the conductive layer and the first plurality of conductive strips in the same pattern to form a second plurality of conductive strips from the conductive layer, the second plurality of conductive trips extending in a first direction, and to form a plurality of floating gates from the first plurality of conductive strips, an individual floating gate having at least a portion of a protrusion and at least a portion of a recess, an individual conductive strip overlying the at least a portion of a protrusion and the at least a portion of a recess of a floating gate (cols. 1-8 and figs. 1-5).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran